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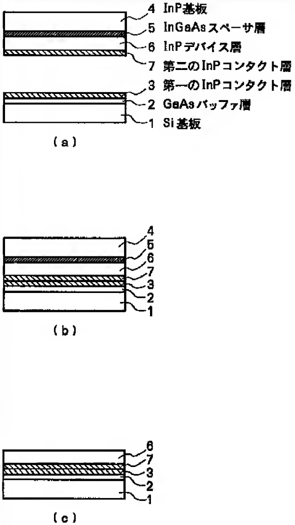
CLAIM + DETAILED DESCRIPTION

[Claim(s)]

[Claim 1]A process of growing up the first In system III-V fellows compound semiconductor contact layer on both sides of the direct or first III-V fellows compound semiconductor layer on the first semiconductor substrate, A process of growing up the second In system III-V fellows compound semiconductor contact layer on both sides of the direct or second III-V fellows compound semiconductor layer on the second semiconductor substrate, A manufacturing method of compounded type semiconductor laminated structure having at least the process on said first and the second semiconductor substrate of carrying out

Drawing selection

Representative drawi



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lamination structures sticking by pressure, via the said first and second In system III-V fellows compound semiconductor contact layers.

[Claim 2]A process of growing up the first In system III-V fellows compound semiconductor layer on both sides of the direct or first III-V fellows compound semiconductor layer on the first semiconductor substrate, A process of growing up the second In system III-V fellows compound semiconductor layer on both sides of the direct or second III-V fellows compound semiconductor layer on the second semiconductor substrate, A process which V fellows element is thermally evaporated from the said first and second In system III-V fellows compound semiconductor layers, and is changed into first and second In system metallic-contacts layers, respectively, A manufacturing method of compounded type semiconductor laminated structure having at least the process of sticking the lamination structures on said first and the second semiconductor substrate by pressure via said first and second In system metallic-contacts layers.

[Claim 3]A manufacturing method of compounded type semiconductor laminated structure characterized by the first and second In system III-V fellows compound semiconductor layers being [both] InP layers in a manufacturing method of the compounded type semiconductor laminated structure according to claim 2.

[Claim 4]. In a manufacturing method of the compounded type semiconductor laminated structure according to claim 2, hold first and second In system metallic-contacts layers more than a melting point. . Or give supersonic vibration to said first and second In system metallic-contacts layers. Or a manufacturing method of compounded type semiconductor laminated structure sticking the lamination structures on said first and the second semiconductor substrate by pressure carrying out melting of the said first and second In system metallic-contacts layers by using these means together.

[Claim 5]. [in a manufacturing method of the compounded type semiconductor laminated structure according to claim 2] [change / into In system metallic-contacts layer / only either of the first or second In system III-V fellows compound semiconductor layer] Or a manufacturing method of compounded type semiconductor laminated structure sticking the lamination structures on said first and

the second semiconductor substrate by pressure after only either of the said first or second In system III-V fellows compound semiconductor layer growing and changing into In system metal layer contact layer.
[Claim 6]A process of growing up the first In system III-V fellows compound semiconductor contact layer and an III-V fellows compound semiconductor device layer one by one on both sides of the direct or first III-V fellows compound semiconductor layer on the first semiconductor substrate, A process of pasting up a supporting board on said III-V fellows compound semiconductor device layer, A process of removing the first semiconductor substrate and the first III-V fellows compound semiconductor layer, and exposing the first In system III-V fellows compound semiconductor contact layer surface, A process of growing up the second In system III-V fellows compound semiconductor contact layer on both sides of the direct or second III-V fellows compound semiconductor layer on the second semiconductor substrate, . [via the first In system III-V fellows compound semiconductor contact layer that said surface exposed, and said second In system III-V fellows compound semiconductor contact layer] A manufacturing method of compounded type semiconductor laminated structure having at least the process of sticking the lamination structures on said supporting board and said second semiconductor substrate by pressure.
[Claim 7][a process of pasting up a supporting board in a manufacturing method of the compounded type semiconductor laminated structure according to claim 6 on an III-V fellows compound semiconductor device layer of the lamination structure top layer formed on the first semiconductor substrate] A process of growing up the third In system III-V fellows compound semiconductor contact layer on said III-V fellows compound semiconductor device layer, A process of growing up the fourth In system III-V fellows compound semiconductor contact layer immediately after on both sides of the third III-V fellows compound semiconductor layer on said supporting board, A manufacturing method of compounded type semiconductor laminated structure comprising at least a process of sticking the lamination structures on said first semiconductor substrate and a supporting board by pressure via the said third and fourth In system III-V fellows compound

semiconductor contact layers.
[Claim 8][a process of pasting up a supporting board in a manufacturing method of the compounded type semiconductor laminated structure according to claim 6 on an III-V fellows compound semiconductor device layer of the lamination structure top layer formed on the first semiconductor substrate] A process of forming an organic adhesive substance layer in at least one surface of said III-V fellows compound semiconductor device layer and said supporting board, A manufacturing method of compounded type semiconductor laminated structure comprising at least a process of sticking lamination structure and said supporting boards on said first semiconductor substrate by pressure via said organic adhesive substance layer.
[Claim 9]In a manufacturing method of the compounded type semiconductor laminated structure according to claim 1, 2, or 6, A manufacturing method of the first, the second semiconductor substrate, and compounded type semiconductor laminated structure, wherein a supporting board is either an III-V fellows compound semiconductor substrate or a group IV semiconductor board further in Claim 6, respectively.
[Claim 10]A process of forming the group IV device layer on the first group IV semiconductor board, and a process of providing an opening which the group IV semiconductor crystal surface exposed in part, A process of growing up the first In system III-V fellows compound semiconductor contact layer on both sides of the direct or first III-V fellows compound semiconductor buffer layer on said group IV semiconductor crystal surface exposed to said opening, A process of growing up an III-V fellows compound semiconductor device layer and the second In system III-V fellows compound semiconductor contact layer on both sides of the direct or second III-V fellows compound semiconductor buffer layer on the second group IV semiconductor board, A process of forming MESA by etching using a mask pattern formed in island shape, Said first In system III-V fellows compound semiconductor contact layer after removing said mask pattern, And a manufacturing method of compounded type semiconductor laminated structure having at least the process of sticking the lamination structures on the said first and second group IV semiconductor boards by pressure via the second In system III-V fellows compound semiconductor contact layer

that remains in said MESA upper part.
[Claim 11]In a manufacturing method of Claim 1 or the compounded type semiconductor laminated structure according to claim 6, 7, or 10, A manufacturing method of compounded type semiconductor laminated structure which an In system III-V fellows compound semiconductor contact layer is InSb an InP layer, an InAs layer, or a layer, and carries out the feature of sticking the lamination structures on two semiconductor substrates by pressure, heating at not less than 300 **.
[Claim 12]In a manufacturing method of Claim 1 or the compounded type semiconductor laminated structure according to claim 6, 7, or 10, A manufacturing method of compounded type semiconductor laminated structure which an In system III-V fellows compound semiconductor contact layer is an InSb layer, and is characterized by sticking the lamination structures on two semiconductor substrates by pressure, carrying out short-time heating melting of said InSb layer with the melting point of not less than 525 **.
[Claim 13]In a manufacturing method of Claim 1 or the compounded type semiconductor laminated structure according to claim 6, 7, or 10, [irradiating with light of a wavelength which an In system III-V fellows compound semiconductor contact layer is an InSb layer, and may be absorbed by only said InSb layer] A manufacturing method of compounded type semiconductor laminated structure sticking the lamination structures on two semiconductor substrates by pressure carrying out heating melting only of said InSb layer with a melting point of not less than 525 **.
[Claim 14]In a manufacturing method of the compounded type semiconductor laminated structure according to claim 6, 7, or 10, After changing said In system III-V fellows compound semiconductor contact layer into In system metallic-contacts layer by a method of evaporating V fellows element thermally after growing up an In system III-V fellows compound semiconductor contact layer, A manufacturing method of compounded type semiconductor laminated structure sticking the lamination structures on two semiconductor substrates by pressure via said In system metallic-contacts layer.

[Detailed Description of the Invention]

[0001]
[Industrial Application]This invention relates to the manufacturing method of the compounded type semiconductor laminated structure which has a quality III-V fellows compound semiconductor single crystal layer on group IV or an III-V fellows lattice mismatching board.
[0002]
[Description of the Prior Art]Now, the trial which forms the III-V fellows compound semiconductor single crystal thin film represented by GaAs and InP on the heteroepitaxial growth on group IV or an III-V fellows lattice mismatching board and the group IV semiconductor single crystal board especially represented by Si is performed actively. This is because an III-V fellows compound semiconductor highly efficient element can be produced on an inexpensive Si substrate and improved efficiency, such as an optical element, can be expected by the high thermal conductivity of Si, when such a thin film structure can be formed. It is because Si super-high integrated circuit, an III-V fellows compound semiconductor very high speed device, and an optical element can be formed on the same board, so development of a new highly efficient element is predicted.
[0003]By the way, in order to apply the III-V fellows compound semiconductor thin film formed on the Si substrate to element production, improvement in crystal quality is important. for example, the Lth of No. 6 with a magazine "Japanese Journal of Applied Physics (Jpn.J.Appl. Phys.)" of volume [24th] (1985), if "two-step growth" currently explained to 391 - 393 pages is used, The single domain single crystal film to which the phase of arrangement of III fellows and V fellows was equal in all the substrate sides is obtained certainly, and crystallinity also improves compared with the conventional direct growth. This is the method of growing up a single crystal film with the usual growing temperature after depositing a thin polycrystal or an amorphous buffer layer first at low temperature, and while carrying out temperature up, a low temperature buffer layer is annealed and single-crystal-izes. However, when GaAs is grown up on a Si substrate, many transposition and stacking faults occur far, and further, the part is easily extended to the upper layer, and serves as penetration dislocation rather than predicted by the Si/GaAs interface from the rate of lattice mismatching. The dislocation density in the case of being based on a two-step

grown method is about 10^8cm in the growth surface of several micrometer thickness. - 2 is also reached.
[0004]Then, the strained layer superlattice intermediate layer and the heat cycle annealing method were introduced, It is about 10^6cm by these. - Dislocation density has improved quickly to 2 (the 24 - 26th page of No. 1 with a magazine "applied physics letter (Appl.Phys.Lett.)" of volume [54th] (1989)). However, about 10^6cm - The result which is less than 2 is not obtained easily, The problem of the thermal expansion coefficient difference of a Si substrate and an III-V fellows compound semiconductor was pointed out as the cause (the 2225 - 2227th page of No. 22 with a magazine "applied physics letter (Appl.Phys.Lett.)" of volume [56th] (1990)). That is, at growing temperature (650 **), it is 10^5cm by introduction of a heat cycle annealing, etc. - Although dislocation density is decreasing below to 2, It is 10^6cm by a stress according to a thermal expansion coefficient difference to under cooling after growth (about 450 ** or less). - Transposition of 2 stand is introduced. the transposition to which much these remains near an interface with a Si substrate -- heat -- it thinks for therefore going up distorted.
[0005]The above problems have more remarkable lattice constant difference with Si at the InP growth on 8% and large Si, Dislocation density is still about 10^7cm· - It is as high as 2 (the 365 - 370th page of the 99th volume (1990) of a magazine "journal OBU Crystal Glaus (J. Crystal Growth)"). Since it becomes a factor to which multiplication of a defect is invited and which reduces a life remarkably also when high-density current is poured into the light-emitting device produced when remains **** was large, it is a problem.
[0006]Other methods of on the other hand laminating the material from which a lattice constant etc. differ include the method of pasting up different-species boards directly, and, as for the method of pasting up Si substrates, research is done already briskly directly. GaAs and InP are recently directly pasted up by heat treatment also about an III-V fellows compound semiconductor, The result of having produced the semiconductor laser of an InP system on the GaAs substrate was reported (the 1961 - 1963rd page of No. 18 with a magazine "applied physics letter (Appl.Phys. Lett.)" of volume [58th] (1991)). In this case, although the transposition based on the lattice mismatching of GaAs and

InP occurs in a joining interface, since the direction of a Burgers vector is edge dislocation parallel to an interface, it is shut up by only the interface, and does not penetrate to an up-and-down crystal layer.
[0007]The example of the method of pasting up Si and a compound semiconductor substrate, unifying and producing a substrate is indicated to JP,S61-182215,A, JP,S61-183915, A, and JP,H2-194519,A.
[0008]
[Problem to be solved by the invention]The problem of the above-mentioned conventional technology adopted in order to obtain a quality III-V fellows compound semiconductor single crystal layer on group IV or an III-V fellows lattice mismatching board is considered.
[0009]By the method of carrying out heteroepitaxial growth of the III-V fellows compound semiconductor single crystal layer directly, there is a problem that remains **** is large on group IV or an III-V fellows lattice mismatching board as mentioned above by the growth on large Si of a thermal expansion coefficient difference whose dislocation density is still especially high.
[0010]They are idea **** when theoretically satisfactory about crystal quality, since the transposition based on lattice mismatching is shut up by only the joining interface in the method of pasting up different-species boards directly on the other hand.
[0011]By the way, at the conventional technology on which said GaAs and InP are directly pasted up by heat treatment, heat treatment of the hot and comparatively long time of 30 minutes was needed at 650 **. Although the report of about 450 ** that low-temperature heat treatment also pasted up directly comparatively was also carried out very much recently ("Proceedings of Workshop of the Institute of Electronics, Information and Communication Engineers" OQE92-147 (1992)), 700 ** high temperature was too needed for pressing down the electric resistance in an interface low enough.
[0012]In order to paste up Si and III-V crystals, such as GaAs and InP, since not less than about 1000 ** high temperature is required for the good adhesion in which the interface void disappeared in adhesion of Si(s), needing further hot heat treatment rather than adhesion of GaAs and InP in this case is predicted.
[0013]Now, when it is going to form Si integrated circuit

and an III-V fellows compound semiconductor element on the same board, after Si integrated circuit pattern is already completed, it is necessary to form an III-V fellows compound semiconductor layer with the process temperature of 400 ** or less. This is because the III-V fellows compound semiconductor layer which serves as conductive impurities to Si in front of not less than 800 ** Si high temperature process, and is easy to carry out mutual thermal diffusion cannot be formed. It is because it is desirable to form an III-V fellows compound semiconductor layer after even aluminum multilayer interconnection of about three layers is usually completed to harness the established existing Si process as it is. In this case, if the melting point of aluminum and the reaction of aluminum and Si are taken into consideration, it is about 400 ** or less, and it is necessary to form an III-V fellows compound semiconductor layer. Therefore, since the direct heteroepitaxial growth in the conventional high temperature and the method of pasting up high temperature lead to destruction of Si integrated circuit directly, it is inapplicable.
[0014]There is also a possibility of big heat distortion occurring during cooling since the thermal expansion coefficient difference is large if heat treatment temperature is high, and also causing generating and multiplication of a defect.
[0015]It is in the purpose of this invention providing the method of manufacturing the compounded type semiconductor laminated structure which has a quality III-V fellows compound semiconductor single crystal layer on group IV or an III-V fellows lattice mismatching board by low-temperature-izing temperature which conquers the fault of such conventional technology and a process takes.
[0016]
[Means for solving problem]The process of growing up the first In system III-V fellows compound semiconductor contact layer on both sides of the direct or first III-V fellows compound semiconductor layer on the first semiconductor substrate according to the invention of Claim 1, The process of growing up the second In system III-V fellows compound semiconductor contact layer on both sides of the direct or second III-V fellows compound semiconductor on the second semiconductor substrate, The manufacturing method of the compounded type semiconductor laminated structure

having at least the process of sticking the lamination structures on said first and the second semiconductor substrate by pressure via the said first and second In system III-V fellows compound semiconductor contact layers is obtained.

[0017]The process of growing up the first In system III-V fellows compound semiconductor layer on both sides of the direct or first III-V fellows compound semiconductor layer on the first semiconductor substrate according to the invention of Claim 2, The process of growing up the second In system III-V fellows compound semiconductor layer on both sides of the direct or second III-V fellows compound semiconductor layer on the second semiconductor substrate, The process which V fellows element is thermally evaporated from the said first and second In system III-V fellows compound semiconductor layers, and is changed into first and second In system metallic-contacts layers, respectively, The manufacturing method of the compounded type semiconductor laminated structure having at least the process of sticking the lamination structures on said first and the second semiconductor substrate by pressure via said first and second In system metallic-contacts layers is obtained. In the process stuck by pressure, first and second In system metallic-contacts layers are held more than a melting point, or supersonic vibration is given to said first and second In system metallic-contacts layers, or these means are used together. Said first and second In system metallic-contacts layers, carrying out melting Or said first, And. [change / only either of the first or second In system III-V fellows compound semiconductor layer / into In system metallic-contacts layer / it / in sticking the lamination structures on the second semiconductor substrate by pressure] Or after only either of the said first or second In system III-V fellows compound semiconductor layer growing and changing into In system metallic-contacts layer, the lamination structures on said first and the second semiconductor substrate are stuck by pressure.

[0018]According to the invention of Claim 6, on both sides of the direct or first III-V fellows compound semiconductor layer, on the first semiconductor substrate The first In system III-V fellows compound semiconductor contact layer, The process of growing up an III-V fellows compound semiconductor device layer one by one, and the process of pasting up a supporting board on said III-V

fellows compound semiconductor device layer, The process of removing the first semiconductor substrate and the first III-V fellows compound semiconductor layer, and exposing the first In system III-V fellows compound semiconductor contact layer surface, On the second semiconductor substrate, direct, . [on both sides of the second III-V fellows compound semiconductor layer] [or via the second In system III-V fellows compound semiconductor contact layer and said second In system III-V fellows compound semiconductor contact layer] The manufacturing method of the compounded type semiconductor laminated structure having at least the process of sticking the lamination structures on said supporting board and said second semiconductor substrate by pressure is obtained. The process at which the process of pasting up a supporting board grows the third In system III-V fellows compound semiconductor contact layer on said III-V fellows compound semiconductor device layer, The process of growing up the fourth In system III-V fellows compound semiconductor contact layer on both sides of the direct or third III-V fellows compound semiconductor layer on said supporting board, It comprises at least a process of sticking the lamination structures on said first semiconductor substrate and a supporting board by pressure via the said third and fourth In system III-V fellows compound semiconductor contact layers. The process at which the process of considering a supporting board as adhesion forms an organic adhesive substance layer in at least one surface of said III-V fellows compound semiconductor device layer and said supporting board, It comprises at least a process of sticking the lamination structure and said supporting boards on said first semiconductor substrate by pressure via said organic adhesive substance layer.
[0019]As mentioned above, according to this invention, the manufacturing method of compounded type semiconductor laminated structure, wherein the first and the second semiconductor substrate, and also a supporting board are either an III-V fellows compound semiconductor substrate or a group IV semiconductor board, respectively is obtained.
[0020]The process of forming the group IV device layer on the first group IV semiconductor board according to the invention of Claim 10, On the process of providing the opening which the group IV semiconductor crystal surface

exposed in part, and said group IV semiconductor crystal surface exposed to said opening, direct, Or the process of growing up the first In system III-V fellows compound semiconductor contact layer on both sides of the first III-V fellows compound semiconductor buffer layer, On the second group IV semiconductor board, direct, Or the process of growing up an III-V fellows compound semiconductor device layer and the second In system III-V fellows compound semiconductor contact layer on both sides of the second III-V fellows compound semiconductor buffer layer, The process of forming MESA by etching using the mask pattern formed in island shape, After removing said mask turn, said first In system III-V fellows compound semiconductor contact layer, And the manufacturing method of the compounded type semiconductor laminated structure having at least the process of sticking the lamination structures on the said first and second group IV semiconductor boards by pressure via the second In system III-V fellows compound semiconductor contact layer that remains in said MESA upper part is obtained.
[0021]As mentioned above, according to this invention, while an In system III-V fellows compound semiconductor contact layer is InSb an InP layer, an InAs layer, or a layer and heats at not less than 300 **, the lamination structures on two semiconductor substrates are stuck by pressure. [what is irradiated with the light of the wavelength which an In system III-V fellows compound semiconductor contact layer is an InSb layer, and carries out short-time heating melting of said InSb layer with the melting point of not less than 525 **, and may be absorbed by only said InSb layer] The manufacturing method of the compounded type semiconductor laminated structure sticking the lamination structures on two semiconductor substrates by pressure is obtained carrying out heating melting only of said InSb layer with the melting point of not less than 525 **.
[0022]In this invention, or after growing up an In system III-V fellows compound semiconductor contact layer, Or after changing said In system III-V fellows compound semiconductor contact layer into In system metallic-contacts layer, the manufacturing method of the compounded type semiconductor laminated structure sticking the lamination structures on two semiconductor substrates by pressure via said In system metallic-contacts layer is obtained.

[0023]
[Function]As a mechanism of direct adhesion, a hydrophilic surface is formed of a surface treatment with sulfuric acid system liquid, and it is thought that it pastes up weakly first, a drying condensation reaction occurs in the process in which it subsequently heat-treats, and it pastes up strongly by the hydrogen bond of OH bases which adsorbed here. Therefore, if combination with oxygen uses the substrate which uses a weaker atom as a component, a drying condensation reaction can occur at low temperature more, and can reduce heat treatment temperature. That is, the direction where the direction of about 600 ** GaAs used In system compound semiconductors, such as InP as which low temperature may be more sufficient than about 500 more ** or less, InAs, and InSb, can paste up at low temperature more rather than Si which needs not less than 850 ** high temperature for evaporation of a surface natural oxidation film.
[0024]Although surface evenness is important for acquiring high adhesion without a void, and a good electrical property, In order that at least 500 ** or less of mass migration by migration may break out by In system compound semiconductor compared with Si which needs not less than 1000 ** high temperature for atomic surface migration, and GaAs which needs not less than 650 **, this fills some crevices between interfaces.
[0025]In In system compound semiconductor, adhesion at low temperature is more possible as mentioned above. Then, if thin In system compound semiconductor layer is beforehand formed in the adhesion surface even when pasting up III-V fellows compound semiconductors other than other group IV or In system,-izing of all the adhesion temperature can be carried out [low temperature].
[0026]Also in In system compound semiconductor, in InSb, at 525 **, the melting point of aluminum, and since it is lower than 660 **, melting and adhesion of the melting point can be carried out by processing of **** short time, such as a flash annealing, in an instant, and it can suppress the influence on Al wiring etc. to the minimum.
[0027]The energy band gap of InSb is the smallest in 0.18 eV, group IV, and an III-V fellows compound semiconductor, and its melting point is also the lowest. Then, if it irradiates with the light of the suitable wavelength

absorbed by only InSb, only InSb can be heated, and it can fuse and can also paste up. (Above, manufacturing method of an invention of Claim 1).

[0028]What is necessary is just to insert the metal of a low melting point into an interface, for enabling adhesion at low temperature. Since [that its elastic modulus is small and also] the metal In has the melting point very as low as about 157 **, it is especially ideal. Even when pasting up Si and an III-V fellows compound semiconductor with a large thermal expansion coefficient difference, if the metal In is inserted, the advantage that **** is absorbable about 100% by a metal In intermediate layer liquefied to near a melting point is during cooling after heat treatment.

[0029]Although it is a formation method of this metal In layer, In system semiconductor layer is convertible for In system metal layer by desorbing V fellows element from In system semiconductor crystal layer. It uses that desorption of P from the surface or As takes place very easily in In system crystals, such as InP and InAs, and the desorption-rate constant of figures triple [2-] is [desorption of P from an InP surface] also especially large compared with desorption of As from Ga system crystal, for example, the GaAs surface. . Change at least one side into a metal In layer among the thin InP layers formed in two material list sides to join. Or what is necessary is to press down heating in melting point of not less than 157 ** of In, or giving supersonic vibration, and to just be stuck by pressure via a metal In layer, after forming a thin InP layer only in one side between two material list sides to join and changing into a metal In layer (manufacturing method of an invention of Claim 2).

[0030]When using the surface of the thick epitaxial growth layer on a crystal substrate for the adhesion surface, the case where sufficient surface evenness is not securable because of generating of a surface defect, degradation of morphology, etc. can be considered. In such a case, what is necessary is to paste up the supporting board on the surface side of an epitaxial growth layer first, to expose the flat interface near the crystal substrate next, and just to use as a final adhesion side. What is necessary is just to use the organic adhesive substance which is based on the manufacturing method of this invention as a method of pasting up a supporting board, or can be equal to next heat treatment, for example, polyimide etc.

[0031]When pasting together the lamination structures on a Si substrate and an InP substrate and a thermal expansion coefficient difference is large, if high temperature heat treatment is performed, the curvature after cooling will pose a problem. The position gap under heat treatment to make the specific position on an InP substrate equivalent to the specific position on a Si substrate, and paste up poses a problem. Also in this case, if a supporting board is used, the thermal expansion coefficient can be arranged similarly to another substrate (manufacturing method of an invention of Claim 6).
[0032]Considering the case where Si super-high integrated circuit uses the pasting-up method for the part on the already formed Si substrate, and forms an III-V fellows compound semiconductor layer in it. The process which 3-4 inches is the maximum and was consistent in the InP substrate or the GaAs substrate cannot be constructed to a 6-8-inch large caliber board being normal as a Si substrate now, but it is inefficient. Then, it is efficient if it pastes up using the III-V fellows compound semiconductor layer which carried out heteroepitaxial growth on another large caliber Si substrate. The Si substrate which used this method for growth the Si super-high integration circuit board side and after adhesion at low temperature although defective ****** in a hetero epitaxial layer remained as a technical problem can be removed, and **** generated in high temperature growth can be removed (manufacturing method of an invention of Claim 10).
[0033]
[Working example]Hereafter, the work example of this invention is described in detail with reference to Drawings.
[0034](Work example 1) Drawing 1 (a) The sectional view in each stairs showed the manufacturing process as an example of an invention of Claim 1 to - (c).
[0035]As shown in drawing 1 (a), the first InP contact layer 3 of 2 or 0.5 micrometer of GaAs buffer layer thickness of 0.5-micrometer thickness is first grown up on Si substrate 1. The second InP contact layer 7 of 6 or 0.5 micrometer of InP device layer thickness of 5 or 2 micrometers of InGaAs spacer layer thickness of 0.5-micrometer thickness is grown up on InP substrate 4. For growth, as III fellows organic metal materials, triethylgallium (TEG), The metal-organic chemical vapor deposition (the MOCVD method) using Al

Singh (AsH_3) and phosphine (PH_3) as triethyl aluminum (TEA) and trimethylindium (TMIn), and a V group material was used.
[0036]Next, as shown in drawing 1 (b), after performing the surface treatment by sulfuric acid system liquid and HF, The lamination structure on Si substrate 1 and InP substrate 4 was piled up on the surfaces via the first InP contact layer 3 and the second InP contact layer 7, light weight was carried, and heat treatment was performed for 30 minutes at 500 ** among hydrogen. The lamination structure on both boards was joined in this process.
[0037]Finally, as shown in drawing 1 (c), by polish and selective etching, InP substrate 4 and the InGaAs spacer layer 5 are removed, and the surface of the InP device layer 6 is exposed.
[0038]The photoluminescence (PL) measurement performed in order to investigate the crystal quality of the obtained InP device layer showed that **** which luminescence intensity without the growth layer and inferiority on an InP substrate is obtained, and originates in the shift of a luminous wavelength, i.e., the thermal expansion coefficient difference of InP/Si, was also small. Dislocation density is also 10^4cm as a result of TEM observation. - It turned out that very good crystal quality is acquired below by 2.
[0039](Work example 2) Drawing 2 (a) A sectional view in each stage showed a manufacturing process as an example of an invention of Claim 2 to - (c).
[0040]As shown in drawing 2 (a), first InP layer 21 of 2 or 0.5 micrometer of GaAs buffer layer thickness of 0.5-micrometer thickness is first grown up on Si substrate 1. Second InP layer 25 of 24 or 0.5 micrometer of GaAs device layer thickness of 23 or 2 micrometers of AlAs spacer layer thickness of 0.5-micrometer thickness is grown up on GaAs substrate 22. The gas source molecular-beam-epitaxial-growth method (MBE technique) for having used Al Singh (AsH_3) and phosphine (PH_3) was used for growth as a V group material.
[0041]Next, as shown in drawing 2 (b), it heats to a suitable temperature of 600 ** or less and not less than 450 **, and P is desorbed from the first InP layer 21 and second InP layer 25, and it changes into the first metal In layer 26 and the second metal In layer 27.

[0042]Next, as shown in drawing 2 (c), the lamination structure on Si substrate 1 and GaAs substrate 22 is stuck by pressure via the first metal In layer 26 and the second metal In layer 27 above the melting point of In, and about 157 **. Finally, by polish and selective etching, GaAs substrate 22 and the AlAs spacer layer 23 are removed, and the surface of the GaAs device layer 24 is exposed.

[0043]Also in the crystal quality of the GaAs device layer obtained by this example, PL measurement and TEM observation showed that there were no growth layer and inferiority on a GaAs substrate. In this example stuck by pressure via a metal In layer, it turned out that there is also no shift of a luminous wavelength and distortion is eased completely.

[0044]In work example 1, although **** remains, in order that it may form a covalent bond interface, very strong adhesive strength is obtained. By the method of on the other hand sticking by pressure via the metal In layer of the work example 2, the adhesive strength can ease distortion of that falling completely.

[0045](Work example 3) Drawing 3 (a) The sectional view in each stage showed the manufacturing process as an example of an invention of Claim 6 to - (e).

[0046]As shown in drawing 3 (a), For example, the third InP contact layer 33 of second 32 or 0.5 micrometer of InGaAs spacer layer thickness of 6 or 0.5 micrometer of InP device layer thickness of first 3 or 2 micrometers of InP contact layer thickness of first 31 or 0.5 micrometer of InGaAs spacer layer thickness of 0.5-micrometer thickness is first grown up on InP substrate 4. A gas source MBE technique was used for growth. The fourth InP contact layer 35 of 0.5-micrometer thickness is grown up on the InP supporting board 34. The second InP contact layer 7 of 0.5-micrometer thickness is grown up on GaAs substrate 22.

[0047]Next, as shown in drawing 3 (b), after performing a surface treatment by sulfuric acid system liquid and HF, Lamination structure on InP substrate 4 and the InP supporting board 34 was piled up on the surfaces via the third InP contact layer 33 and the fourth InP contact layer 35, light weight was carried, and heat treatment was performed for 30 minutes at 500 ** among hydrogen. Lamination structure on both boards was joined in this process.

[0048]Next, as shown in drawing 3 (c), polish and selective etching remove InP substrate 4 and the first InGaAs spacer layer 31, and the following table side of the first InP contact layer 3 is exposed.
[0049]Next, as shown in drawing 3 (d), after performing the surface treatment by sulfuric acid system liquid and HF, The lamination structure on GaAs substrate 22 and the InP supporting board 34 was piled up on the surfaces via the second InP contact layer 7 and the first InP contact layer 3, light weight was carried, and heat treatment was performed for 30 minutes at 500 ** among hydrogen. The lamination structure on both boards was joined in this process.
[0050]Finally, as shown in drawing 3 (e), by polish and selective etching, the InP supporting board 34, the fourth InP contact layer 35, the third InP contact layer 33, and the second InGaAs spacer layer 32 are removed, and the surface of the InP device layer 6 is exposed.
[0051]The projections of the diameter of a maximum of 1-2 micrometer according to a crystal defect or adhesion garbage in the surface of the top layer of multilayer structure grown-up on InP substrate 4 by this example and the third InP contact layer 33 are tens - hundreds of piece cm· - It was distributed by the density of 2. Therefore, in junction of the lamination structures on InP substrate 4 of drawing 3 (b), and the InP supporting board 34, the void remained in the interface, and adhesive strength was also weak. However, there was almost no projection in the following table side of the first InP contact layer 3 exposed by polish and selective etching by drawing 3 (c), and what also has sufficiently strong adhesive strength was obtained, without a void remaining in an interface also subsequent junction.
[0052]Also in the crystal quality of the InP device layer obtained by this example, PL measurement and TEM observation showed that there were no growth layer and inferiority on an InP substrate.
[0053](Work example 4) Drawing 4 (a) The sectional view in each stage showed the manufacturing process as another example of an invention of Claim 6 to - (e).
[0054]As shown in drawing 4 (a), For example, first InP layer 21 of second 32 or 0.5 micrometer of InGaAs spacer layer thickness of 6 or 0.5 micrometer of InP device layer thickness of first 3 or 2 micrometers of InP contact layer thickness of first 31 or 0.5 micrometer of InGaAs spacer

layer thickness of 0.5-micrometer thickness is first grown up on InP substrate 4. The gas source MBE technique was used for growth.
[0055]Second InP layer 25 of 2 or 0.5 micrometer of GaAs buffer layer thickness of 0.5-micrometer thickness is grown up on the Si supporting board 41.
[0056]The second InP contact layer 7 of 24 or 0.5 micrometer of GaAs device layer thickness of 2-micrometer thickness is grown up on Si substrate 1.
[0057]Next, as shown in drawing 4 (b), it heats to a suitable temperature of 600 ** or less and not less than 450 **, and P is desorbed from the first InP layer 21 and second InP layer 25, and it changes into the first metal In layer 26 and the second metal In layer 27.
[0058]Next, as shown in drawing 4 (c), the lamination structure on InP substrate 4 and the Si supporting board 41 is stuck by pressure via the first metal In layer 26 and the second metal In layer 27 with the melting point of not less than about 157 ** of In. By polish and selective etching, InP substrate 4 and the first InGaAs spacer layer 31 are removed, and the following table side of the first InP contact layer 3 is exposed.
[0059]Next, as shown in drawing 4 (d), after performing the surface treatment by sulfuric acid system liquid and HF, The lamination structure on Si substrate 1 and the Si supporting board 41 was piled up on the surfaces via the second InP contact layer 7 and the first InP contact layer 3, light weight was carried, and heat treatment was performed for 30 minutes at 500 ** among hydrogen. The lamination structure on both boards was joined in this process.
[0060]Finally, as shown in drawing 4 (e), by polish and selective etching, the Si supporting board 41, GaAs buffer layer 2, the second metal In layer 27, the first metal In layer 26, and the second InGaAs spacer layer 32 are removed, and the surface of the InP device layer 6 is exposed.
[0061]Also in the crystal quality of the InP device layer obtained by this example, PL measurement and TEM observation showed that there were no growth layer and inferiority on an InP substrate.
[0062]By the way, since thermal expansion coefficient differences are thick large substrates when the lamination structure on the Si supporting board 41 and InP substrate 4 is pasted up by high temperature heat treatment like the

work example 1, the curvature of the substrate after cooling is not avoided. However, at this example, in order to paste up at low temperature via a metal In layer, there is almost no curvature of a substrate, and there is no bad influence to the following adhesion process.

[0063]Since both substrates are Si(s), the problem of the position gap by the thermal expansion coefficient difference under heat treatment does not produce them to arrange specific horizontal positions with the InP device layer 6 which moved at the 1st adhesion process onto the Si supporting board 41, and the GaAs device layer 24 on Si substrate 1, and paste up.

[0064](Work example 5) Drawing 5 (a) The sectional view in each stage showed the manufacturing process as an example of an invention of Claim 10 to - (d).

[0065]As shown in drawing 5 (a), on first Si substrate 51, the Si device structure layer 52 of the a maximum of 3-micrometer thickness containing aluminum multilayer interconnection layer is formed first, and the opening which the surface of first Si substrate 51 exposed is provided in the part. The first InSb contact layer 53 of 0.5-micrometer thickness is grown up to be the surface of first Si substrate 51 first exposed to this opening. InSb layers other than the surface portion of first Si substrate 51 are removed after growth using the gas source MBE technique which added Sb source cell.

[0066]Next, GaAs buffer layer 2 of 0.5-micrometer thickness is grown up on second Si substrate 54, The first GaAs device layer 55 of 0.7-micrometer thickness is grown up performing a heat cycle annealing (900 ** - 450 **) about twice on the way, Next, the InGaAs/GaAs strained layer superlattice layer 56 ($In_{0.2}Ga_{0.8}As$: 10 nm) GaAs:

Grow up the AlAs spacer layer 23 of 20 nm, x10 cycle, and 0.5-micrometer thickness, grow up the second GaAs device layer 57 of 3-micrometer thickness further, and, finally grow up the second InSb contact layer 58 of 0.5-micrometer thickness.

[0067]Next, a compound semiconductor layer on second Si substrate 54 is etched by using as a mask the SiO_2 film 59 patterned as shown in drawing 5 (b), and MESA is formed. It is made in agreement [a position in the level surface of MESA] with a position of an opening established in first Si

substrate 51. heat according to a thermal expansion coefficient difference at a stage which grew multilayer structure on second Si substrate 54 -- since it is distorted, it has curved in the whole, but it becomes flat by forming MESA.

[0068]Next, as shown in drawing 5 (c), lamination structure on first Si substrate 51 and second Si substrate 54 is piled up by surface said after removing the SiO_2 film 59 via the first InSb contact layer 53 in which it was provided in an opening, and the second InSb contact layer 58 on MESA, Light weight was carried and short-time lamp heating for 5 seconds was performed among hydrogen with a melting point of not less than about 525 ** of InSb. Lamination structure on both boards was joined in this process.

[0069]As finally shown in drawing 5 (d), with polish and selective etching. Second Si substrate 54, GaAs buffer layer 2, the first GaAs device layer 55, the InGaAs/GaAs strained layer superlattice layer 56, and the AlAs spacer layer 23 are removed, and the surface of the second GaAs device layer 57 is exposed.

[0070]As for the crystal quality of the GaAs device layer obtained by this example, in PL measurement, the growth layer on a GaAs substrate and mostly equal luminescence intensity were obtained. The shift of a luminous wavelength is also small and it turned out that heat distortion is eased mostly. This is because second Si substrate 54 was removed to patterning by mesa Shigeru, and **. As a result of TEM observation, there is also much dislocation density and it is 10^4-10^5cm^{-} It turned out that 2 and good crystal quality are acquired.

[0071]In this example, since the compound semiconductor crystals which grew epitaxially directly and were formed on second Si substrate 54 are moved by the pasting-up method onto first Si substrate 51, the usual Si VLSI process using an 8-inch large caliber Si substrate can take consistency as it is, for example.

[0072]Adhesive strength is also strong in order for the influence on Al wiring to be able to stop an InSb contact layer by heat treatment of a **** short time in an instant to the minimum since it pastes up, melting and, and also to form a covalent bond interface fundamentally.

[0073]Although the first InSb contact layer 53 was formed in the opening which the surface of first Si substrate 51

exposed in this example, It may form in the surface which the opening which the surface exposed could be sufficient as as long as the crystal layer existed in the Si device structure layer 52, or was obtained by etching further from the surface of first Si substrate 51.
[0074]Although the first InSb contact layer 53 was formed only in the opening, selective growth may be carried out by the MOCVD method etc. using the SiO_2 mask which forms in the whole surface, and could use only the inside of an opening, and was formed in the surfaces other than the opening surface.
[0075]As the object for MESAETCHINGU, and also a mask for the above-mentioned selective growth, amorphous films, such as Si_3N_4 other than a SiO_2 film (for example, AlN), may be used, in addition organic matters, such as a semiconductor crystal, metal, a resist layer, may be used as an object for MESAETCHINGU.
[0076]Only InSb will be heated if it irradiates with the light of the suitable wavelength which may use other methods for melting of an InSb contact layer, for example, is absorbed by only the InSb layer, the heat can carry out melting, can also paste up, and the influence on Al wiring is suppressed completely, and according to this adhesion process itself -- distorted generating is also avoidable.
[0077]Although the gas source MBE technique or the MOCVD method was used as a grown method in the above five work examples, for example, other halogen conveying methods may be used.
[0078]When sticking an up-and-down layer by pressure via a metal In layer in work examples 2 and 4, it heated in melting point of not less than about 157 ** of In, but the method of giving other supersonic vibration etc. may be used. Although InP->In and conversion used the easy metal In as a metal layer, Ga may be added, for example and it may change with an InGaP->In-Ga alloy. Although desorption of P becomes slow by Ga addition, the melting point of In-Ga alloy can be lowered.
[0079]In the five work examples, when an InP layer or a GaAs layer was formed in up to a Si substrate, explained to the example the case where an InP layer was formed in up to a GaAs substrate etc., but. The group IV boards are germanium and Si_xgermanium$_{1.\ A-x}$ mixed crystal and

Si_xgermanium$_1$ When it has an epilayer of a - x mixed crystal, The case of mixed crystals, such as InAs of others [compound semiconductor layer / which InP, GaP, and a mixed crystal form / an III-V fellows board / in the case of / a compound semiconductor layer / them / III-V fellows], GaP, InGaP, and also when a two or more kinds III-V fellows compound semiconductor layer is intermingled, this invention can be applied widely.
[0080]A different combination from five work examples in all may be adopted as the purpose also about an adhesion method. For example, melting of the InSb contact layer may not be carried out, but it may paste up only by [suitable] carrying out time heat treatment below with a melting point. As an adhesion method of a supporting board in work examples 3 and 4, a heat-resistant organic adhesive substance, for example, polyimide etc., may be used.
[0081]
[Effect of the Invention]According to this invention, the compounded type semiconductor laminated structure which has a quality III-V fellows compound semiconductor single crystal layer on group IV or an III-V fellows lattice mismatching board is realizable at low temperature as mentioned above.

[Translation done.]

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